SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on Japanese Patent Applications No. 2010-158004 filed on Jul. 12, 2011, and No. 2011-112587 filed on May 19, 2011, the disclosures of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates to a semiconductor device having a super junction structure and a manufacturing method of a semiconductor device having a super junction structure.

BACKGROUND

[0003] Conventionally, an avalanche resistance in a trench gate type super junction MOS transistor in a semiconductor device is improved, and the device is disclosed in JP-A-2008-288367 corresponding to US 2008/0283913 and JP-A-2009-43966. In the device, the super junction structure is formed such that a P conductive type region and a N conductive type region are alternately arranged in a substrate having a N conductive type along with a direction in parallel to the surface of the substrate. A P conductive type channel layer is formed in a surface portion of the super junction structure. A N^+ conductive type source region is formed in a surface portion of the channel layer, and the source region is opposite to the N conductive type region in the super junction structure. A contact P^+ conductive type region is formed in a surface portion of the channel layer, and the P^+ conductive type region is opposite to the P conductive type region in the super junction structure. The impurity concentration of the P^+ conductive type region is higher than the P conductive type channel layer. An embedded P^+ conductive type region is formed in the P conductive type channel layer such that the embedded P^+ conductive type region contacts the contact P^+ conductive type region. The impurity concentration of the embedded P^+ conductive type region is higher than the P conductive type channel layer.

[0004] A trench is formed such that the trench penetrates the source region and the channel layer, and reaches the N conductive type region. A gate electrode is formed on an inner wall of the trench via a gate insulation film. Thus, the trench, the gate insulation film and the gate electrode provide the trench gate structure. Here, the embedded P^+ conductive type region is formed between adjacent two trenches.

[0005] In the semiconductor device, an avalanche current generated in the super junction structure is discharged to the contact P^+ conductive type region via the P^+ conductive type region. Specifically, when the break down occurs at the P conductive type region, the avalanche current is flown from the embedded P^+ conductive type region to the contact P^+ conductive type region. Further, when the break down occurs at the N conductive type region, the avalanche current is flown from to the contact P^+ conductive type region via the P conductive type channel layer on the N conductive type region and the embedded P^+ conductive type region, which has the impurity concentration higher than the P conductive type channel layer.

[0006] Accordingly, a parasitic bipolar transistor is restricted from functioning. The parasitic bipolar transistor is driven by flowing the avalanche current through the channel layer on the trench side and the source region. Thus, the avalanche resistance is improved.

[0007] Further, a planar type semiconductor device having a super junction structure is disclosed in JP-A-2002-16250. Specifically, in the device, a P conductive type base region is formed in a surface portion of the P conductive type region in the super junction structure. A N^+ conductive type source region is formed in a surface portion of the base region. A groove is formed on the base region, and the groove reaches the P conductive type region. A poly silicon layer is embedded in the groove via an insulation film. A gate electrode is formed on the surface of each of the base region, the source region and the N conductive type region via a gate insulation film. The gate electrode is disposed at a predetermined region of the surface.

[0008] Further, JP-A-2007-150142 corresponding to US 2007/0132012 teaches that a planar type semiconductor device having a super junction structure, in which a high impurity concentration layer is formed on the surface of a P conductive type region disposed at a corner of a P conductive type base region. The impurity concentration of the high impurity concentration layer is higher than the P conductive type region. Further, the impurity concentration of the high impurity concentration layer is constant, i.e., locally homogeneous.

[0009] However, in JP-A-2002-16250 and JP-A-2007-150142, although the planar type semiconductor device having the super junction structure is disclosed, there is no information about avalanche resistance.

[0010] A semiconductor device including a planar type semiconductor device with a super junction structure is disclosed in JP-A-2004-134714. In the device, an avalanche resistance is improved such that a high impurity concentration layer is formed in a surface portion of a P conductive type region. The impurity concentration of the high impurity concentration layer is higher than the P conductive type region, and is locally homogeneous. In this case, a negative resistance is improved, and the avalanche resistance is also improved. Here, in the device, a base layer is arranged between the high impurity concentration layer and a contact P^+ conductive type region.

[0011] JP-A-2008-288367, JP-A-2009-43966 and JP-A-2004-134714 teaches that the avalanche resistance is improved in the semiconductor device. However, it is required to improve the avalanche resistance much more.

SUMMARY

[0012] In view of the above-described problem, it is an object of the present disclosure to provide a semiconductor device having a super junction structure and a manufacturing method of a semiconductor device having a super junction structure. In the semiconductor device, an avalanche resistance is improved.

[0013] According to a first aspect of the present disclosure, a semiconductor device includes: a substrate having a first conductive type; a plurality of first conductive type regions and a plurality of second conductive type regions disposed on the substrate, extending in a first direction, and alternately arranged in a second direction so that a super junction structure is provided; a channel layer having a second conductive type and disposed on the super junction structure; a first conductive type layer disposed in a first surface portion of the channel layer; a contact second conductive type region dis-